

Final Design Report:

Operational Amplifier Using Folded Cascade with Mirroring Topology

Class: ECE 722

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1. Summary

The purpose of this assignment was to design an operational amplifier using the folded cascode with current mirroring topology given to us. It was built using AMI 0.6 μ m technology. We were to design our circuit to the following specifications: $V_{DD} = 3V$, maximum power usage = 1mW, minimum linear output swing of 1.5V, minimum voltage gain > 300 at 100kHz, and a minimum phase margin of 45°. This report will detail the ECE722 final project and its steps: a brief introduction to the components used, an overall design overview, results, design analysis, and conclusions made.

2. Introduction

Operational amplifiers, or op-amps, are an essential building block of many mixed-mode systems. The folded-cascode op-amp arrangement is a widely used op-amp arrangement in high-frequency switched capacitor filters because it provides a large gain, and is easy to frequency compensate with a load/compensation capacitor. The folded-cascode arrangement has high open-loop voltage gain in the low frequency range that makes it easy to be designed as a high-speed operational amplifier. A current mirror is an arrangement designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. There are three main specifications that characterize a current mirror: 1) the transfer ratio (in the case of a current amplifier) or the output current magnitude (in the case of a constant current source CCS), 2) the AC output resistance, which determines how much the output current varies with the voltage applied to the mirror, 3) the minimum voltage drop across the output part of the mirror necessary to make it work properly. The minimum voltage is dictated by the need to keep the output transistor of the mirror in active

mode. The range of voltages where the mirror works is called the compliance range and the voltage marking the boundary between good and bad behavior is called the compliance voltage.

3. Design Overview

3.1 – Procedure

The following steps were taken in completing this project:

- 1) Design the circuit given to us, seen in Figure #1, in the project description in Cadence, understanding the current divisions needed.

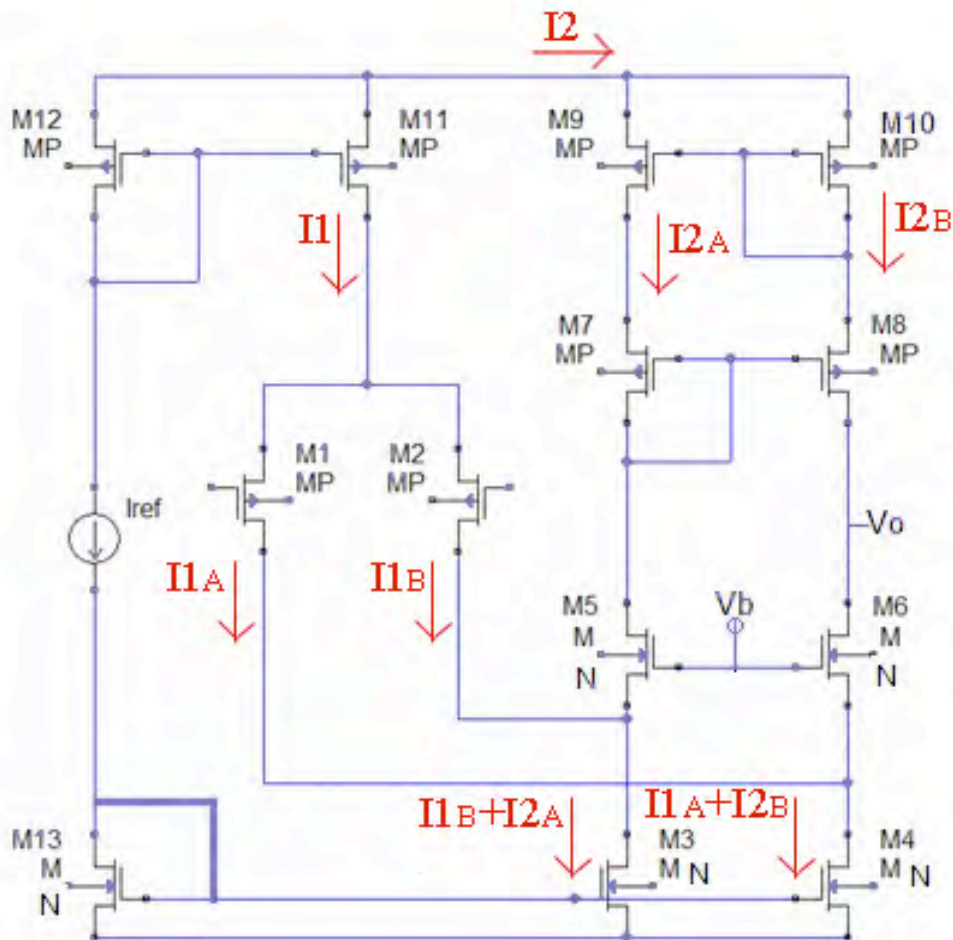


Figure #1: Given circuit, with added currents (marked in red)

- 2) Expand from the given circuit and add wire connections, ground, V_{DD} , V_{CM} , V_{AC} , and C_L .
- 3) The following equations, assumptions, and equation results were used to solve for variable values and current:

$$I_{\max} = \frac{P_{\max}}{V_{DD}} = \frac{1mW}{3V} = 333\mu A \quad (\text{Equation \#1})$$

$$\epsilon_0 = 8.854 \times 10^{-12} \text{ F/m}$$

$$\epsilon_r = 39$$

$$t_{ox} = 1.41 \times 10^{-8} \text{ m}$$

$$r_o = \frac{1}{\lambda * I_D}$$

$$C_{OX} = \frac{\epsilon_0 \epsilon_r}{t_{ox}} = \frac{[(8.854 \times 10^{-12}) * (39)]}{1.41 \times 10^{-8}} = .0244897872 \text{ F/m}^2 \quad (\text{Equation \#2})$$

$$\text{NMOS: } V_{th} = .7086 \text{ V}, \mu_n = 533.6953445$$

$$\text{PMOS: } V_{th} = -.91179952 \text{ V}, \mu_p = 202.4540953$$

$$K_n = \mu_n * C_{OX} = 130.702 \mu A/V^2$$

$$K_p = \mu_p * C_{OX} = 49.581 \mu A/V^2$$

Upper end of swing	Lower end of swing	
$V_{CM} \text{ (common-mode voltage)} = \frac{[(V_{OV5,6} + V_{OV3,4}) + (3 - (V_{OV9,10} + V_{OV7,8}))]}{2}$		(<i>Equation \#3</i>)

$$V_{\text{swing}} \text{ (voltage swing)} = 3 - (2 * V_{OV7-10} + V_{OV5,6} + V_{OV3,4}) \quad (\text{Equation \#4})$$

$$V_b \text{ (voltage bias)} = V_{OV3,4} + V_{OV5,6} + V_{th} \quad (\text{Equation \#5})$$

$$V_{OV} \text{ (over-voltage)} = \sqrt{\frac{2 * I_D}{\mu * C_{OX} * (\frac{W}{L})}} = \sqrt{\frac{2 * I_D}{K * (\frac{W}{L})}} \rightarrow W/L = \frac{2 * I_D}{\mu * C_{OX} * V_{OV}^2} = \frac{2 * I_D}{K * V_{OV}^2} \quad (\text{Equation \#6})$$

$$g_m = \frac{2 * I_D}{V_{GS} - V_{th}} = \frac{2 * I_D}{V_{OV}} \quad (\text{Equation \#7})$$

$$= \mu * C_{OX} * \left(\frac{W}{L}\right) * V_{OV} \quad (\text{Equation \#8})$$

$$= 2 * I_D * \mu * C_{OX} * \left(\frac{W}{L}\right) \quad (\text{Equation \#9})$$

3.2 – Simulations

The final cadence design was simulated with the below situations and values stated in section 3.3:

- 1) Phase/Gain/Transient of the circuit, with no body effect and no unity gain (open loop)
 - a. Transient range
 - b. Measure gain
 - c. Measure phase margin (PM)
 - d. Bandwidth
- 2) Phase/Gain/Transient of the circuit, with body effect and no unity gain (open loop)
 - a. Transient range
 - b. Measure gain
 - c. Measure phase margin (PM)
 - d. Bandwidth
- 3) Phase/Gain/Transient of the circuit, with no body effect and unity gain (closed loop)
 - a. Transient range
 - b. Measure gain
 - c. Measure phase margin (PM)
 - d. Measure bandwidth
 - e. Measure slew rate
- 4) Phase/Gain/Transient of the circuit, with body effect and unity gain (closed loop)
 - a. Transient range
 - b. Measure gain
 - c. Measure phase margin (PM)
 - d. Measure bandwidth

- e. Measure slew rate
- 5) Replace V_{ac} with square wave pulse V_{pulse} , measure with no body effect and use unity gain (closed loop).
- 6) Replace V_{ac} with square wave pulse V_{pulse} , measure with body effect and use unity gain (closed loop).

3.3 – Design Specifications

The following values were chosen for the circuit:

- I_{ref} : 60 μ A
- I1: 240 μ A
 - o I1a: 120 μ A
 - o I1b: 120 μ A
- I2: 30 μ A
 - o I2a: 15 μ A
 - o I2b: 15 μ A
- I1b+I2a: 135 μ A
- I1a+I2b: 135 μ A
- Set Overdrive Voltages (V_{ov})
 - o M3: .15V
 - o M4: .15V
 - o M5: .05V
 - o M6: .05V
 - o M7: .05V

- o M8: .05V
- o M9: .05V
- o M10: .05V
- W/L ratios
 - o M1: $\frac{799.95}{.6} \mu$
 - o M2: $\frac{799.95}{.6} \mu$
 - o M3: $\frac{55.05}{.6} \mu$
 - o M4: $\frac{55.05}{.6} \mu$
 - o M5: $\frac{55.05}{.6} \mu$
 - o M6: $\frac{55.05}{.6} \mu$
 - o M7: $\frac{145.2}{.6} \mu$
 - o M8: $\frac{145.2}{.6} \mu$
 - o M9: $\frac{145.2}{.6} \mu$
 - o M10: $\frac{145.2}{.6} \mu$
 - o M11: $\frac{97.8}{.6} \mu$
 - o M12: $\frac{24.45}{.6} \mu$
 - o M13: $\frac{24.45}{.6} \mu$
- V_b : .9V

- V_{CM} : 1.55V
- V_{swing} : 2.69V

3.4 – Process and Design Explanation

The first step in designing the circuit was to work out the design specifications by deciding on an I_{ref} , current and dividing up the current. As seen in equation #1, if we are given a maximum power of 1mW and a rail voltage of 3V, there is a maximum current of 333 μ A to work with. We can divide up the calculated current amongst the I_{ref} and stated currents I_1 and I_2 , and then estimate the voltage overdrive. M7-10, M5-6, and M3-4 are set first since the rest of the circuit is dependent on their set values. In Figure #2, different test cases are documented in order to find a workable solution. Equations #3, #4, #5, and #6 are used in the chart in Figure #3 in order to find W/L , V_{CM} , V_b , V_{swing} , and then in reverse to confirm I_D and V_{OV} .

	V _{ov}	W/L	V _{ov}	W/L	V _{ov}	W/L	V _{ov}	W/L	V _{ov}	W/L	use 3.5pf	48 deg
I _{ref}	60		60		60		100		50		60	
I ₁	180		180		240		100		200		240	
I _a	90		90		120		50		100		120	
I _b	90		90		120		50		100		120	
I ₂	90		90		30		100		50		30	
I _{2a}	45		45		15		50		25		15	
I _{2b}	45		45		15		50		25		15	
I _{1b} + I _{2a}	135		135		135		100		125		135	
I _{1a} + I _{2b}	135		135		135		100		125		135	
	V _{ov}	W/L	V _{ov}	W/L	V _{ov}	W/L	V _{ov}	W/L	V _{ov}	W/L	V _{ov}	W/L
M _{12,13}		55.05/.6		13.8/.6		55.05/.6		91.8/.6		20.4/.6		24.45/.6
M ₁₁		165.15/.6		41.4/.6		165.15/.6		91.8/.6		81.8/.6		97.8/.6
M _{1,2}		799.95/.6		799.95/.6		799.95/.6		799.95/.6		799.95/.6		799.95/.6
M ₇₋₁₀	.1	108.9/.6	.1	108.9/.6	.1	36.3/.6	.1	121.05/.6	.05	242.2/.6	.05	145.2/.6
M _{5,6}	.1	41.25/.6	.1	41.25/.6	.1	13.8/.6	.1	45.9/.6	.05	91.8/.6	.05	55.05/.6
M _{3,4}	.1	123.9/.6	.2	31.05/.6	.1	123.9/.6	.1	91.8/.6	.15	51/.6	.15	55.05/.6
V _{cm}	1.5		1.55		1.5		1.5		1.55		1.55	
V _b	.9		1		.9		.9		.9		.9	
V _{swing}	2.6		2.5		2.6		2.6		2.7		2.699	
Max Gain:	287.347		253.55		210.95		220.54		322		354.38	
BP:	24.556kHz		25.046kHz		25.672kHz		22.691kHz		10kHz		9.8275kHz	
PM:	18		25		30		29		8		7	

Figure #2: Test Cases

In Figure #3, when the I_D current for each branch was set, the V_{ov} of the specified MOSFETs could be estimated and used to find a theoretical W/L. Due to the measurement set used in Cadence, not all W/L were valid, hence values that were close to or equal to the calculated theoretical W/L were used in Cadence then plugged back into the calculation sheet in order to check original assumptions.

Estimate:	M7-10	M5,6	M3,4	Vswing check		
I_D :	15.0000	15.0000	135.0000		unCox =	130.702
set V_{ov} :	0.0500	0.0500	0.1500	2.7000	upCox =	49.581
set W/L :	242.0000	91.7500	91.7500		Vth =	0.7086
calculated V_{ov} :	0.0500	0.0500	0.1501	2.6999	Iref =	60
calculated W/L :	242.0282	91.8119	91.8119			
W (est. units):	145.2169	55.0871	55.0871			
L (est. units):	0.6000	0.6000	0.6000			
I_D Ratio (with I_{ref}):	1/4	1/4	2 1/4			
Used:						
W :	145.2000	55.0500	55.0500			
L :	0.6000	0.6000	0.6000			
used W/L :	242.0000	91.7500	91.7500			
check V_{ov} of used W/L :	0.0500	0.0500	0.1501			
V_{CM} =	1.5500					
V_b =	0.9087					
V_{swing} =	2.6999					

Figure #3: Calculation Sheet

4. Results

The conditions discussed in section 3.2 were tested and the final measured results are shown in the sections below. The total measured results for gain, phase, bandwidth, transient range, and slew rate are displayed in Figure #4, with the corresponding circuits and graphs displayed in sections 4.1 through 4.6. Their corresponding figure numbers are documented in the results chart.

Figures		Gain (mV)	Phase (deg)	BW (kHz)	Transient (V)	Transient Oscillation Voltage
#5, #6	<i>NoBE_NoUnity</i>	max: 390.23mV	1) -3dB pt: $10^{(-3/20)} \cdot \text{gain}$ = .7079*390.23 = 276.243817 @168.73kHz, 2) 1% pt: $10^{(1/20)}$ = 1.12mV @ 52 MHz	high, low	1.67V, 897.3mV	<--- low, high
		@100k: 335mV	Use 1% pt: -132.5 deg @ 52 MHz	6.9kHz, 105MHz	106.704	<--- first dist.
			47.5		105.83	<--- last dist.
#7, #8	<i>BE_NoUnity</i>	max: 423.86mV	1) -3dB pt: $10^{(-3/20)} \cdot \text{gain}$ = .7079*423.86 = 300.0505mV @ 153.95kHz, 2) 1% pt: $10^{(1/20)}$ = 1.12mV @ 52 MHz	high, low	1.71V, 873mV	<--- low, high
		@100k: 325mV	Use 1% pt: -133 deg @ 52 MHz	4.44kHz, 125MHz	97.115	<--- first dist.
			47		96.95	<--- last dist.
#9, #10	<i>NoBE_Unity (sine)</i>	max: 381.74mV	1) -3dB pt: $10^{(-3/20)} \cdot \text{gain}$ = .7079*381.74 = 270.233746mV @ 144kHz, 2) 1% pt: $10^{(1/20)}$ = 1.12mV @ 45MHz	high, low	1.63V, 892mV	<--- low, high
		@100k: 310mV	Use 1% pt: -139 deg @ 45Mhz	4.5kHz, 125MHz	98.106	<--- first dist.
			41		102.94	<--- last dist.
#11, #12	<i>BE_Unity (sine)</i>	max: 416.93mV	1) -3dB pt: $10^{(-3/20)} \cdot \text{gain}$ = .7079*416.93 = 295.144747mV @ 132.55kHz, 2) 1% pt: $10^{(1/20)}$ = 1.12mV @ 45MHz	high, low	1.65V, 870mV	<--- low, high
		@100k: 312mV	Use 1% pt: -140 deg @ 45MHz	6.75kHz, 125MHz	100.213	<--- first dist.
			40		100.45	<--- last dist.

Figure #4a: Final Results Sheet

Transient (Min, Max in V)							
#13, #14	NoBE_Unity (pulse)	(788.06ps, 1.3213V)	V Total Change	V pt. (@ 10% & 90%)	pt. (@ 10% & 90%) -->	us pt. (@ 10% & 90%)	Slew Rate (V/us)
		(1.2285us, 2.147V)	0.8257	1.40397	36.2189 ns	0.0362189	$S_r = (V_{pt2} - V_{pt1}) / (t_{p2} - t_{pt1})$
				2.06453	134.142 ns	0.134142	6.745701474
				V pt. (@ 0% & 90%)	pt. (@ 0% & 90%) ---->	us pt. (@ 0% & 90%)	Slew Rate (V/us)
				1.3213	788.06 ps	0.00078806	$S_r = (V_{pt2} - V_{pt1}) / (t_{p2} - t_{pt1})$
				2.06453	134.142 ns	0.134142	5.573363637
				V pt. (@ linear slope region)	pt. (@ linear slope region) ---->	us pt. (@ linear slope region)	Slew Rate (V/us)
				1.3213	788.06 ps	0.00078806	$S_r = (V_{pt2} - V_{pt1}) / (t_{p2} - t_{pt1})$
				2.0952	143.531 ns	0.143531	5.421634163
Transient (Min, Max in V)							
#15, #16	BE_Unity (pulse)	(616.93ps, 1.3305V)	V Total Change	V pt. (@ 10% & 90%)	pt. (@ 10% & 90%) -->	us pt. (@ 10% & 90%)	Slew Rate (V/us)
		(1.238us, 2.1508V)	0.8203	1.41273	36.102 ns	0.036102	$S_r = (V_{pt2} - V_{pt1}) / (t_{p2} - t_{pt1})$
				2.06877	139.88 ns	0.13988	6.321571046
				V pt. (@ 0% & 90%)	pt. (@ 0% & 90%) ---->	us pt. (@ 0% & 90%)	Slew Rate (V/us)
				1.3305	616.93 ps	0.00061693	$S_r = (V_{pt2} - V_{pt1}) / (t_{p2} - t_{pt1})$
				2.06877	139.88 ns	0.13988	5.301261849
				V pt. (@ linear slope region)	pt. (@ linear slope region) ---->	us pt. (@ linear slope region)	Slew Rate (V/us)
				1.3305	616.93 ps	0.00061693	$S_r = (V_{pt2} - V_{pt1}) / (t_{p2} - t_{pt1})$
				2.0999	144.2 ns	0.1442	5.358570478

Figure #4b: Final Results Sheet

4.1 – Phase/Gain/Transient of the circuit, with no body effect and no unity gain (open loop)

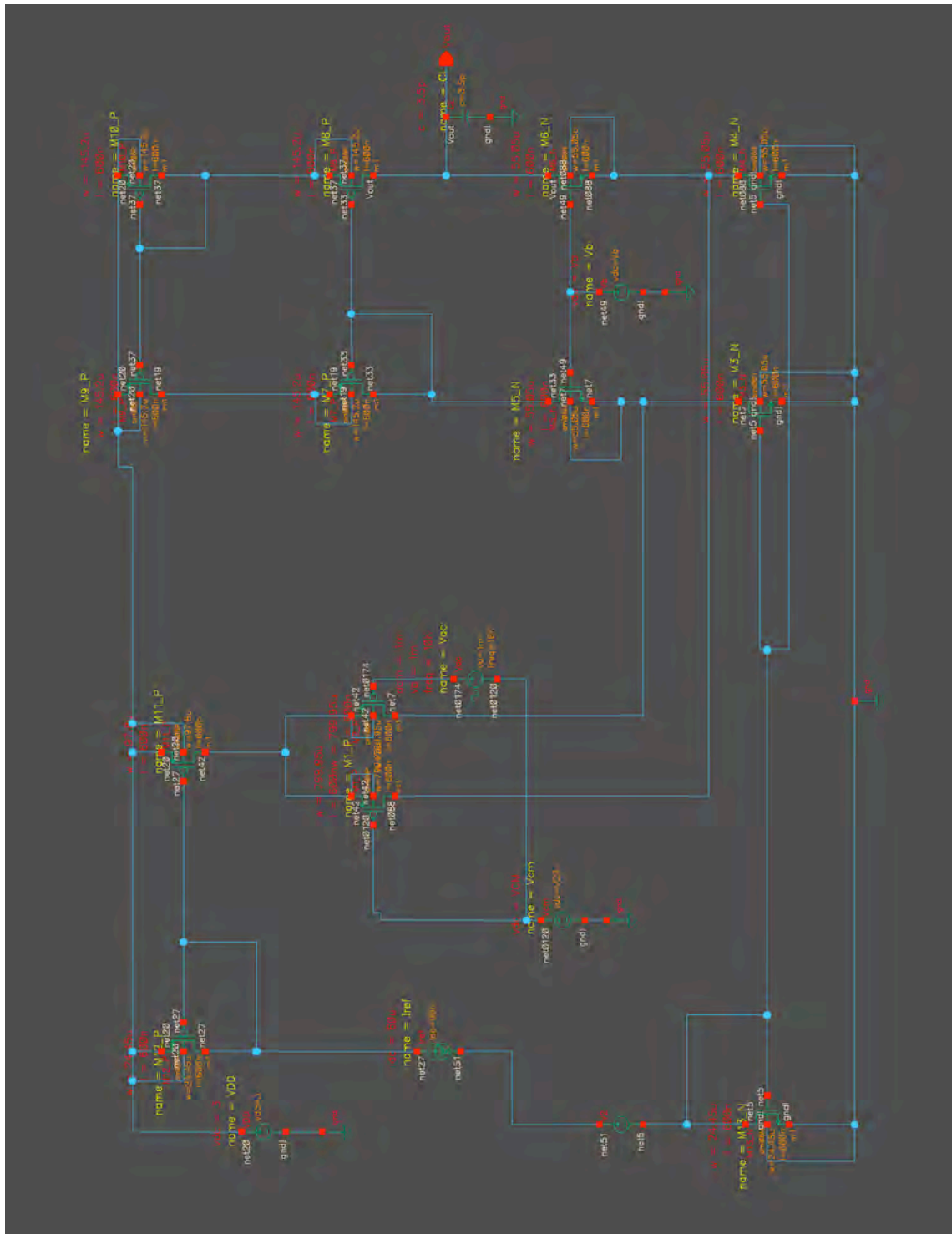


Figure #5: Circuit

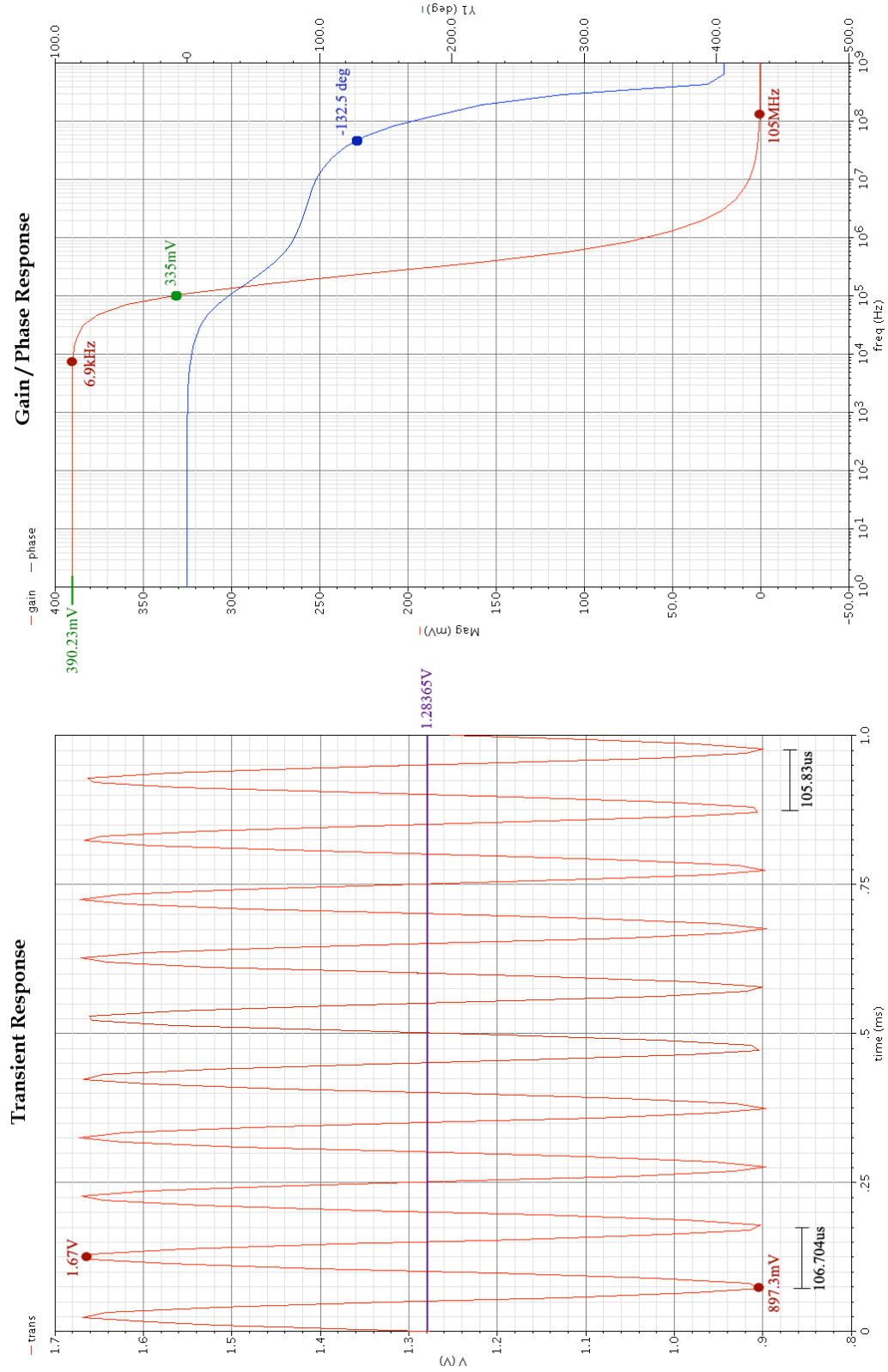


Figure #6: Transient range, Gain, Phase Margin (PM), Bandwidth

4.2 – Phase/Gain/Transient of the circuit, with body effect and no unity gain (open loop)

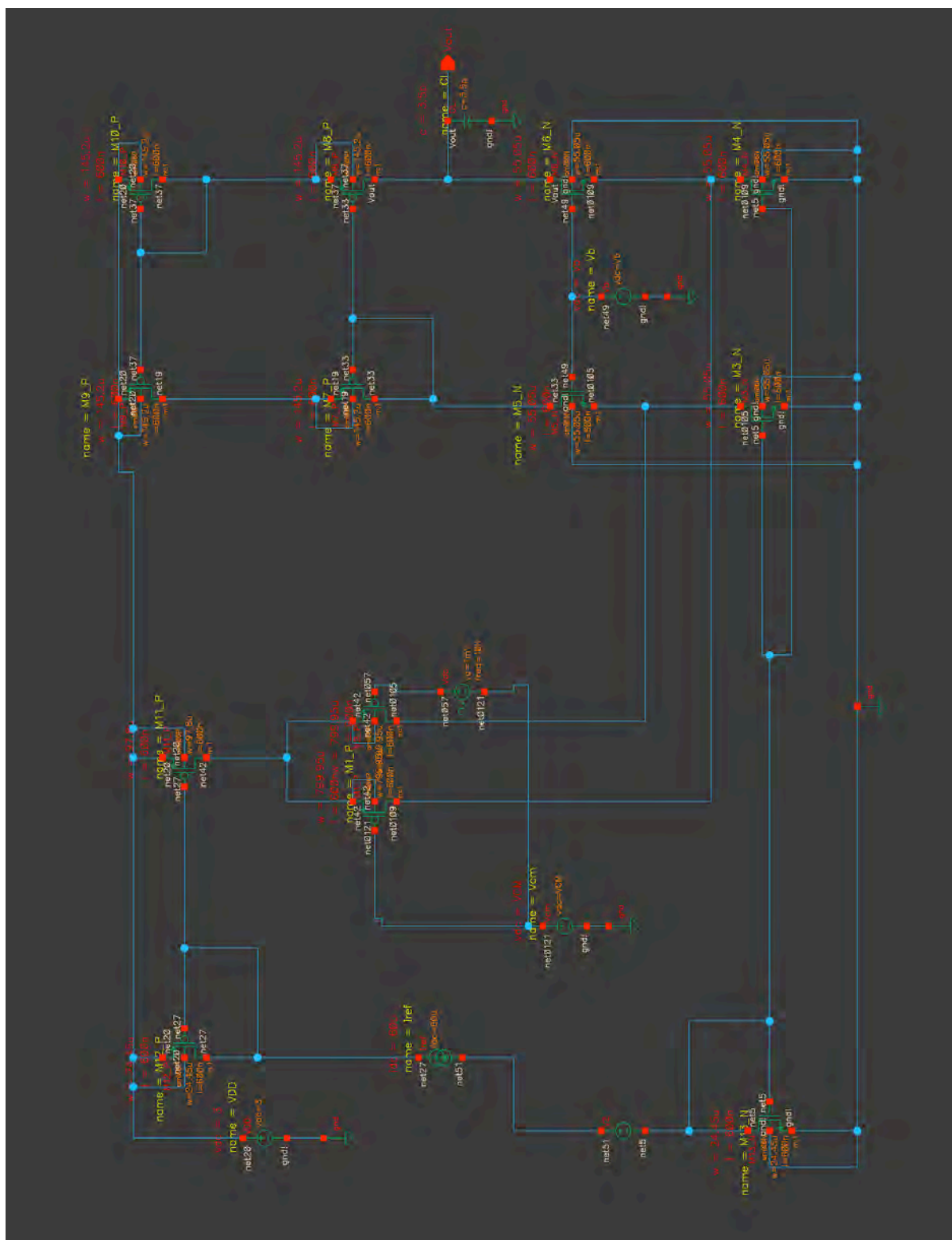


Figure #7: Circuit

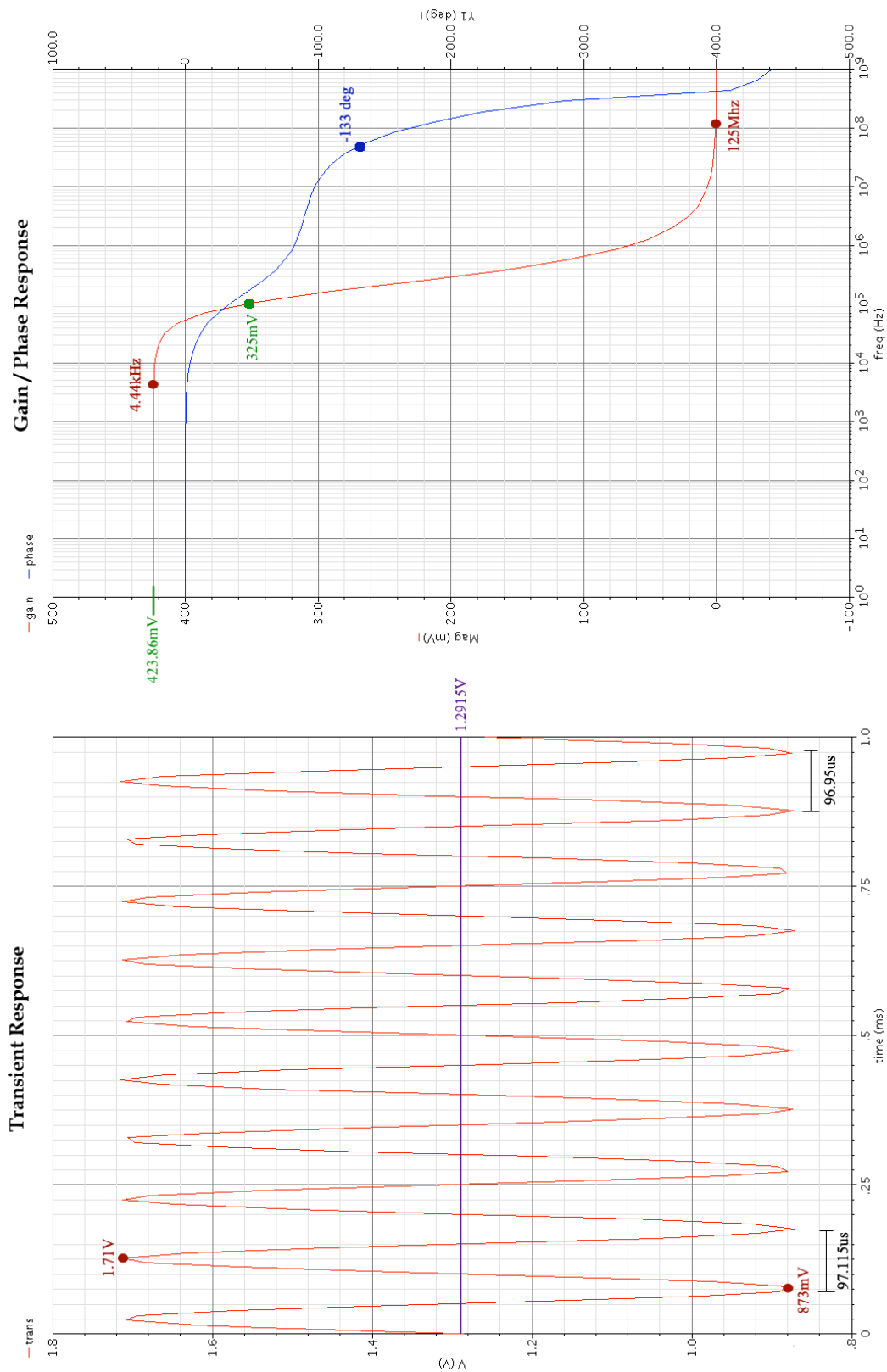


Figure #8: Transient range, Gain, Phase Margin (PM), Bandwidth

4.3 – Phase/Gain/Transient of the circuit, with no body effect and unity gain (closed loop)

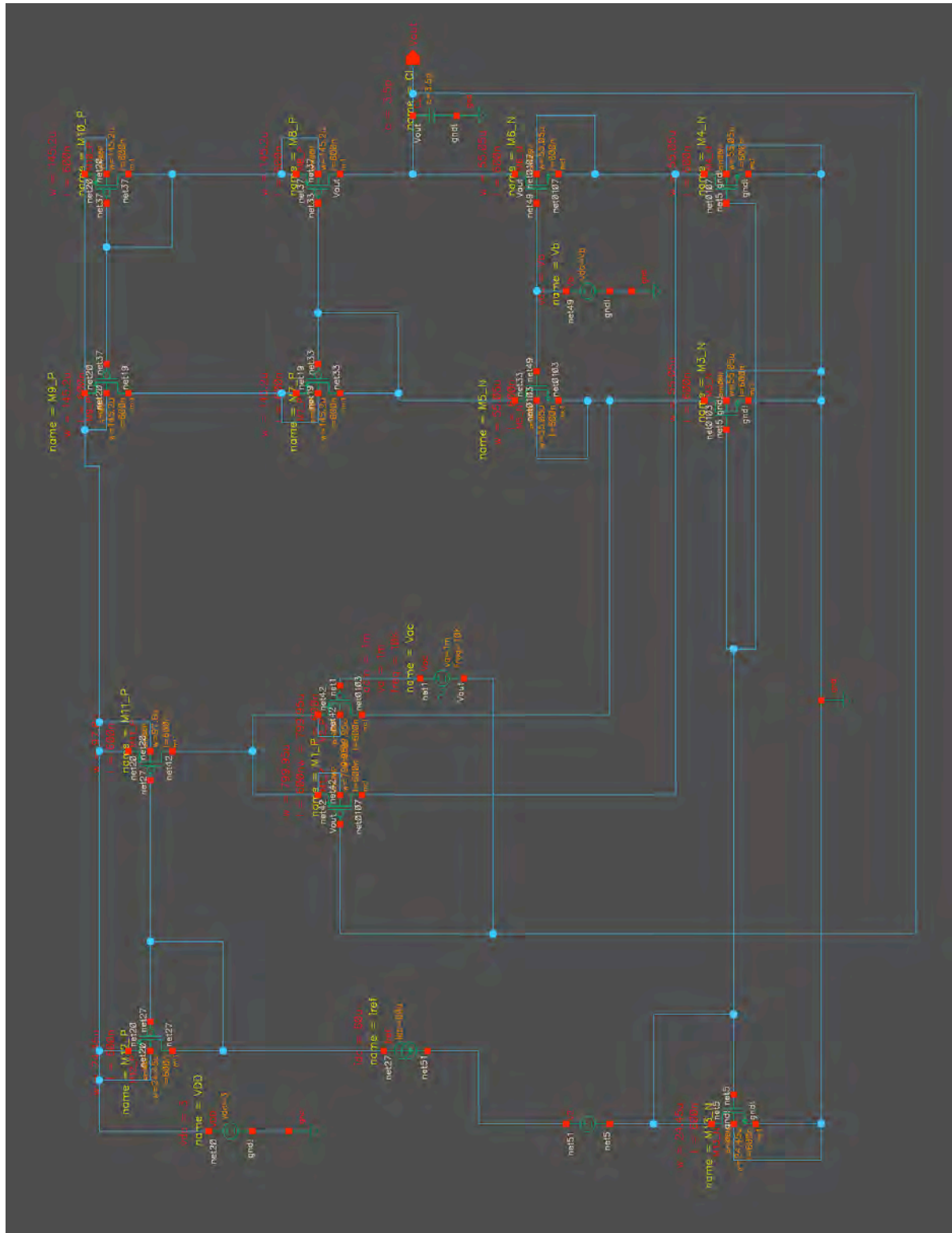


Figure #9: Circuit

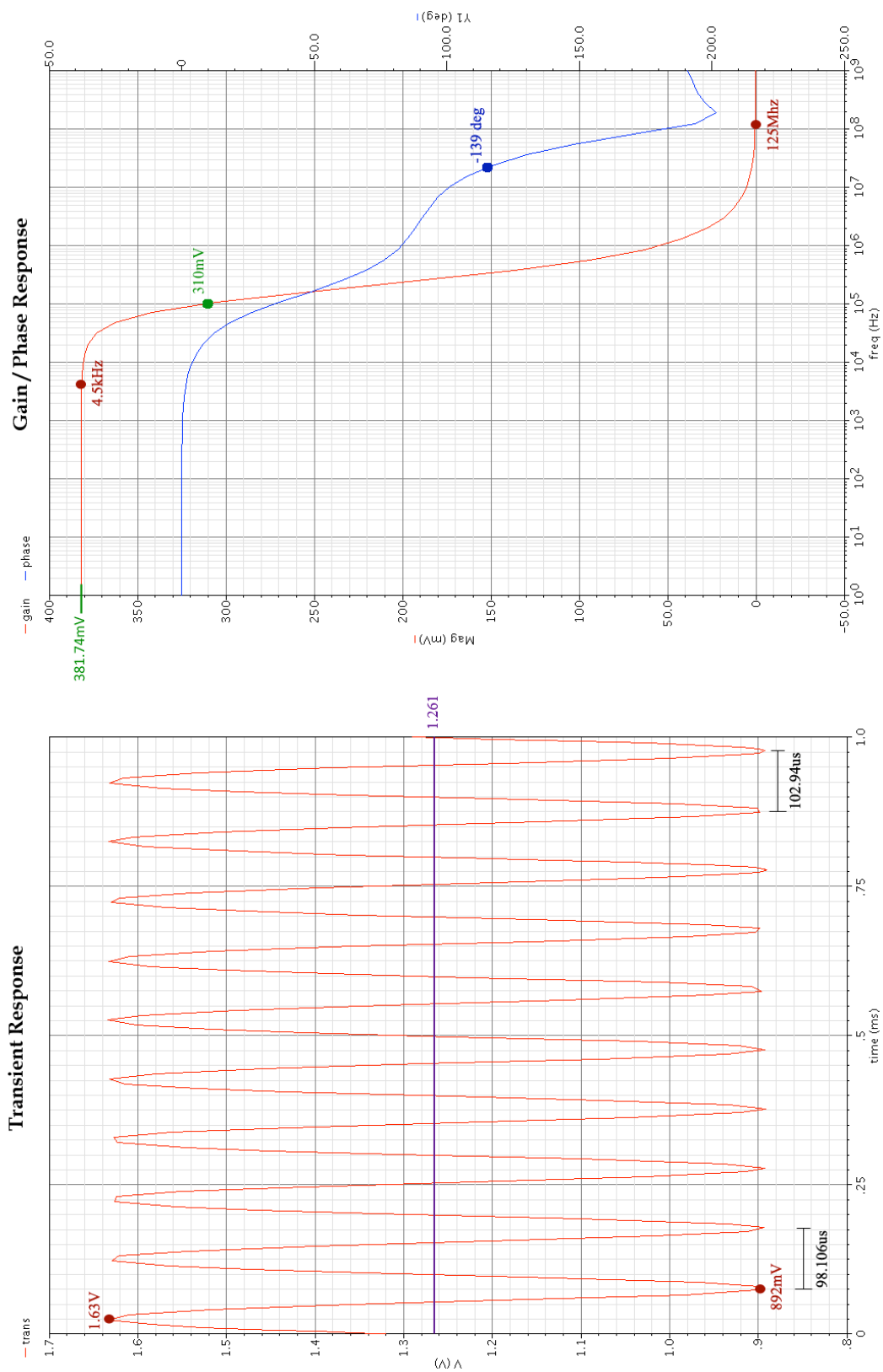


Figure #10: Transient range, Gain, Phase Margin (PM), Bandwidth

4.4 – Phase/Gain/Transient of the circuit, with body effect and unity gain (closed loop)

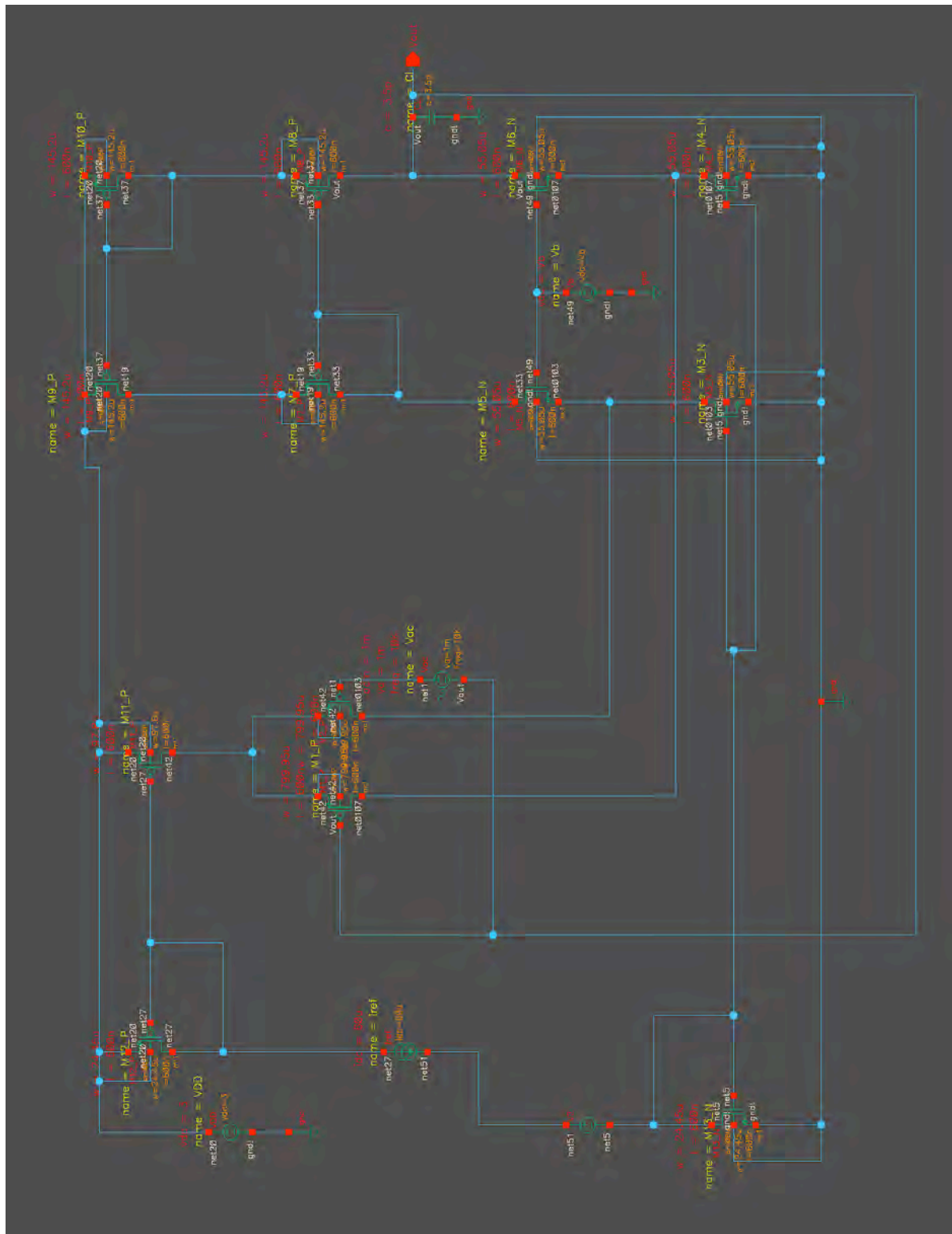


Figure #11: Circuit

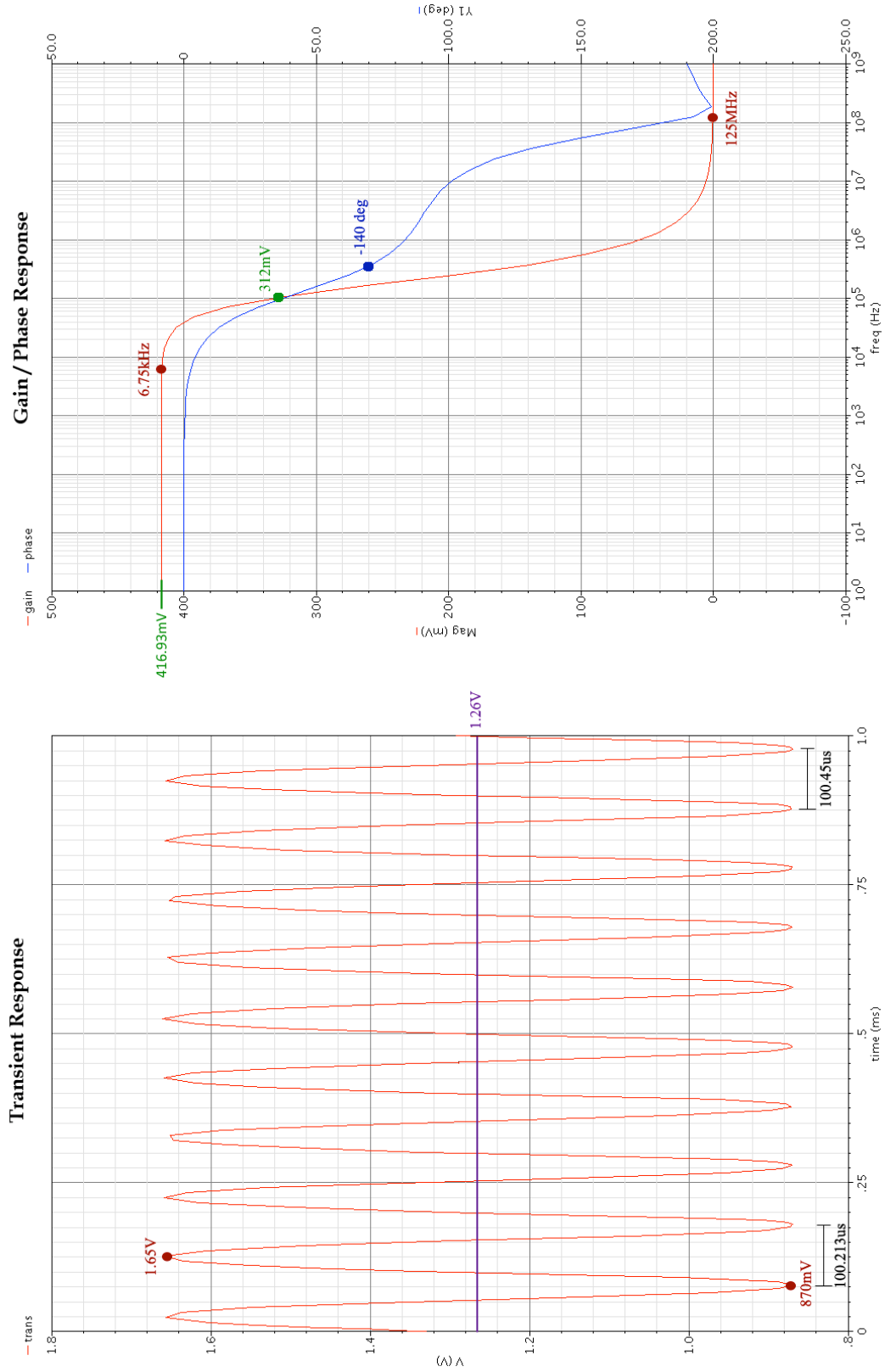


Figure #12: Transient range, Gain, Phase Margin (PM), Bandwidth

4.5 – Phase/Gain/Transient of the circuit, no body effect and unity gain (closed loop), and square wave pulse

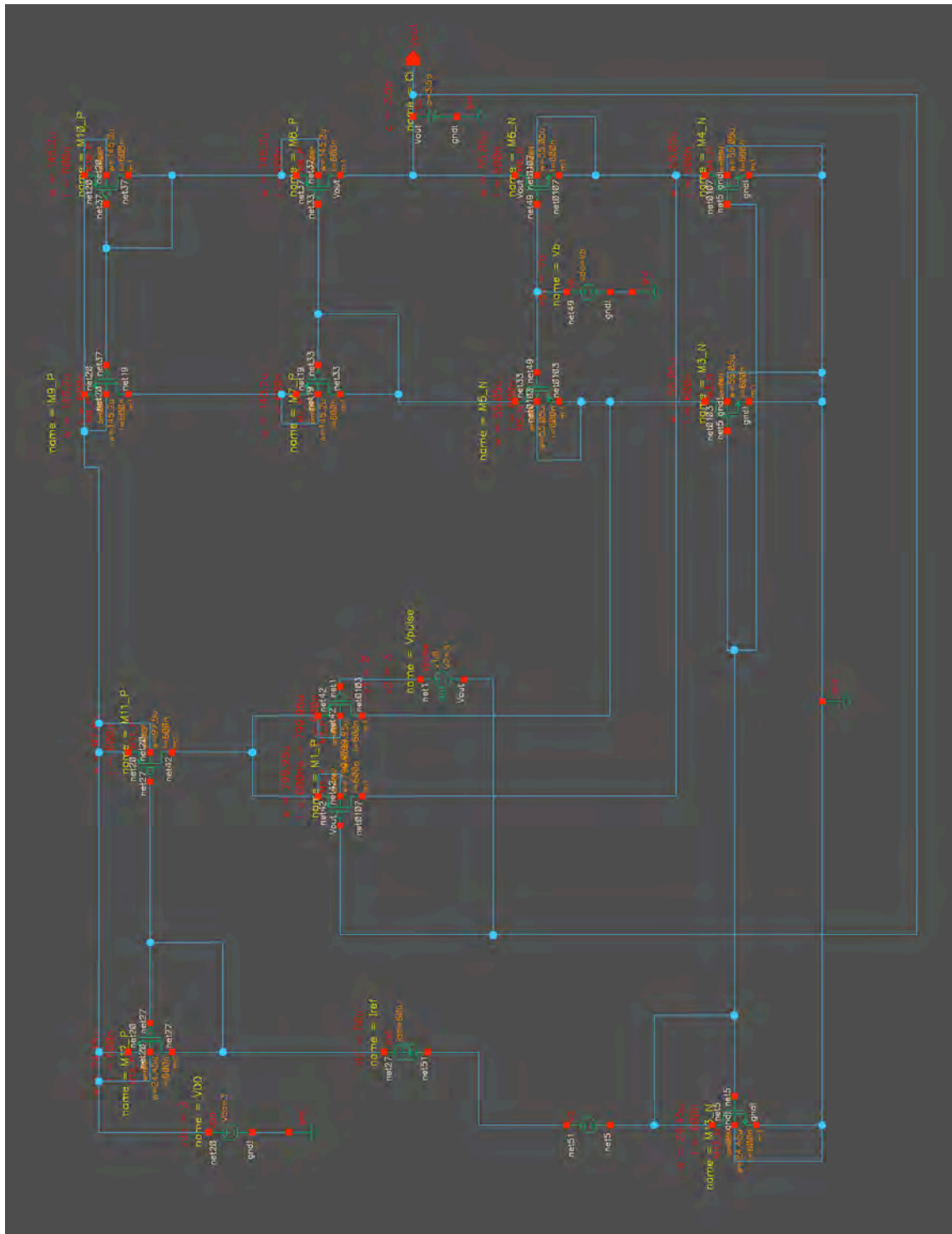


Figure #13: Circuit

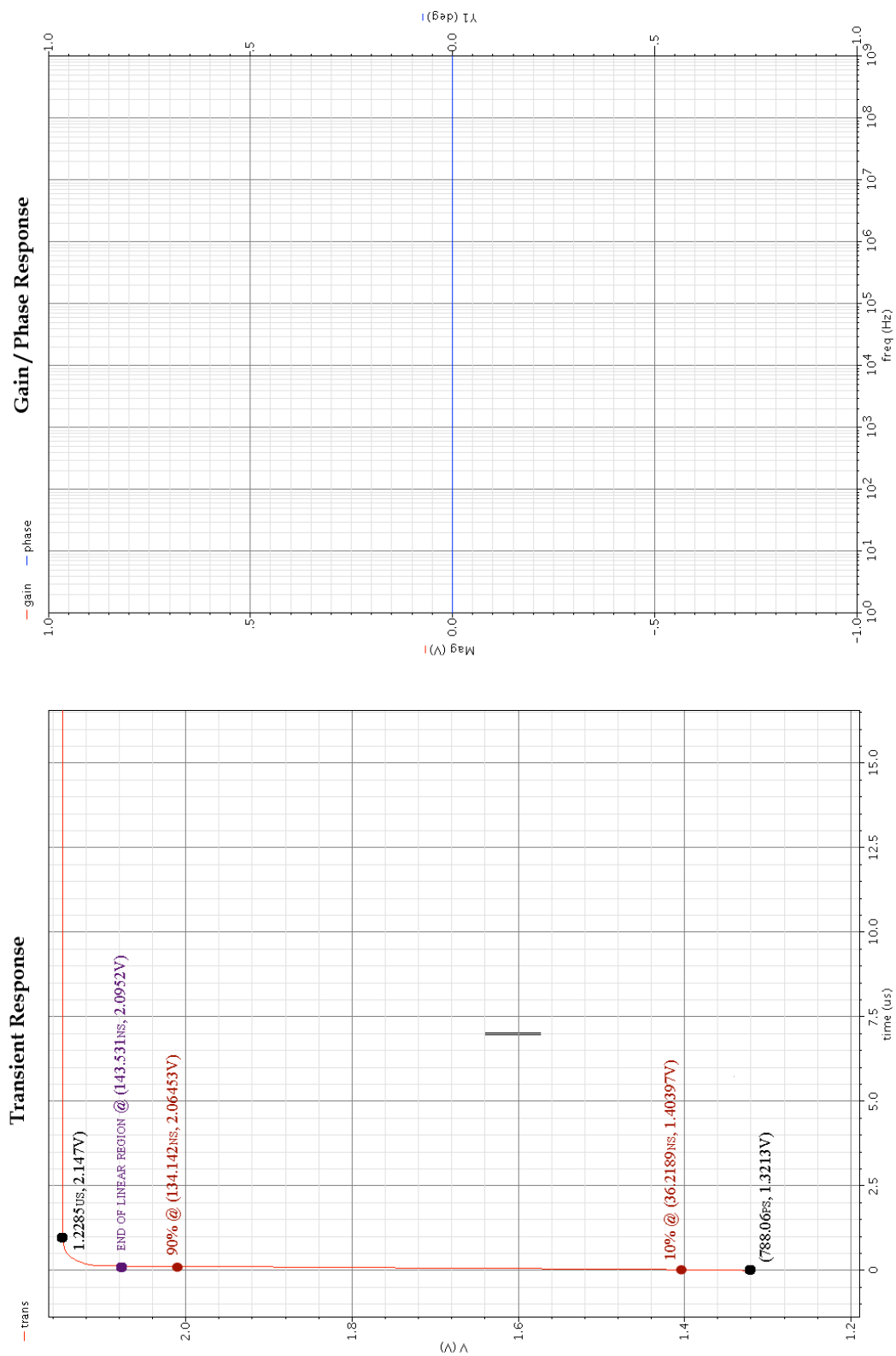


Figure #14: Slew Rate

4.6 – Phase/Gain/Transient of the circuit, body effect and unity gain (closed loop), and square wave pulse

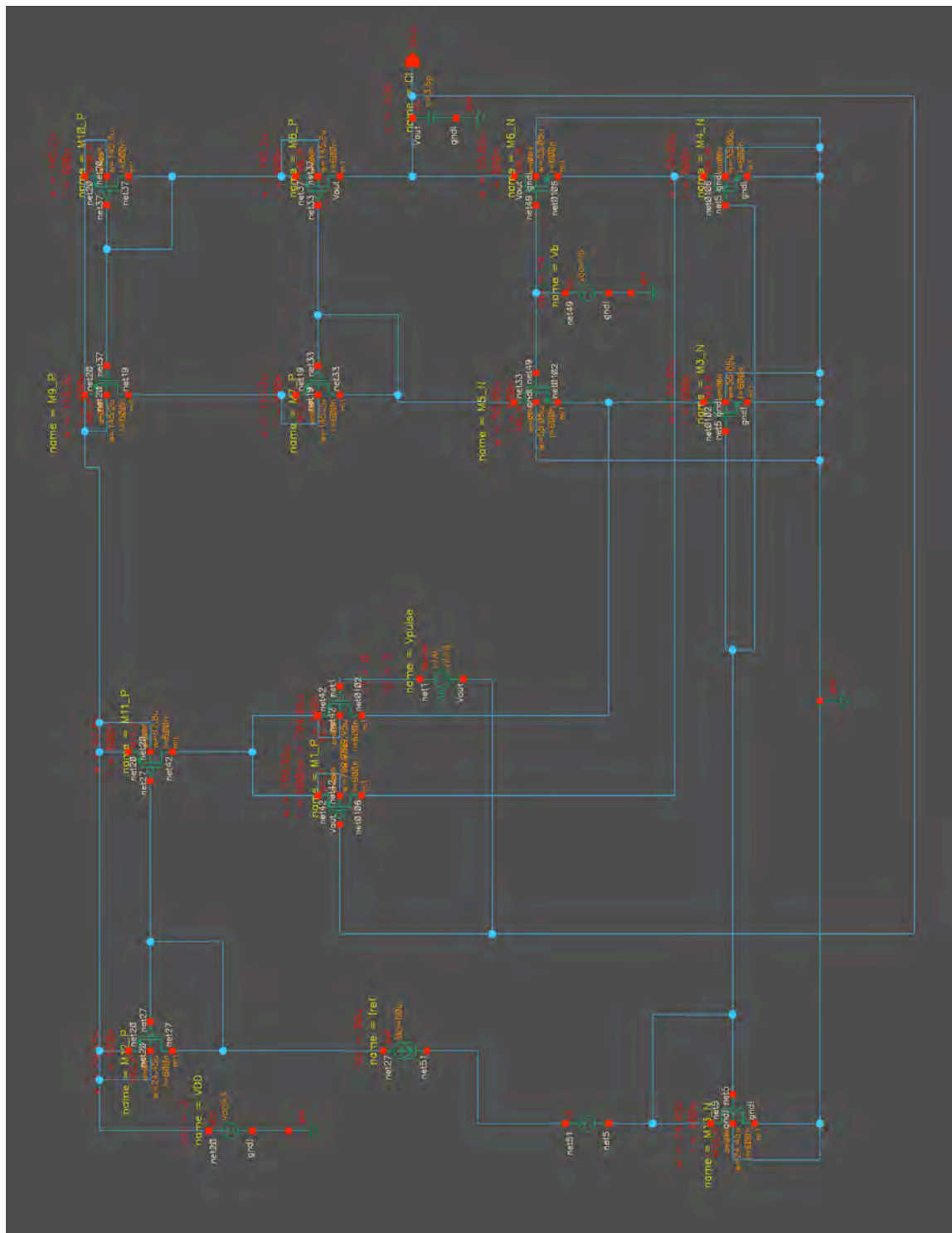


Figure #15: Circuit

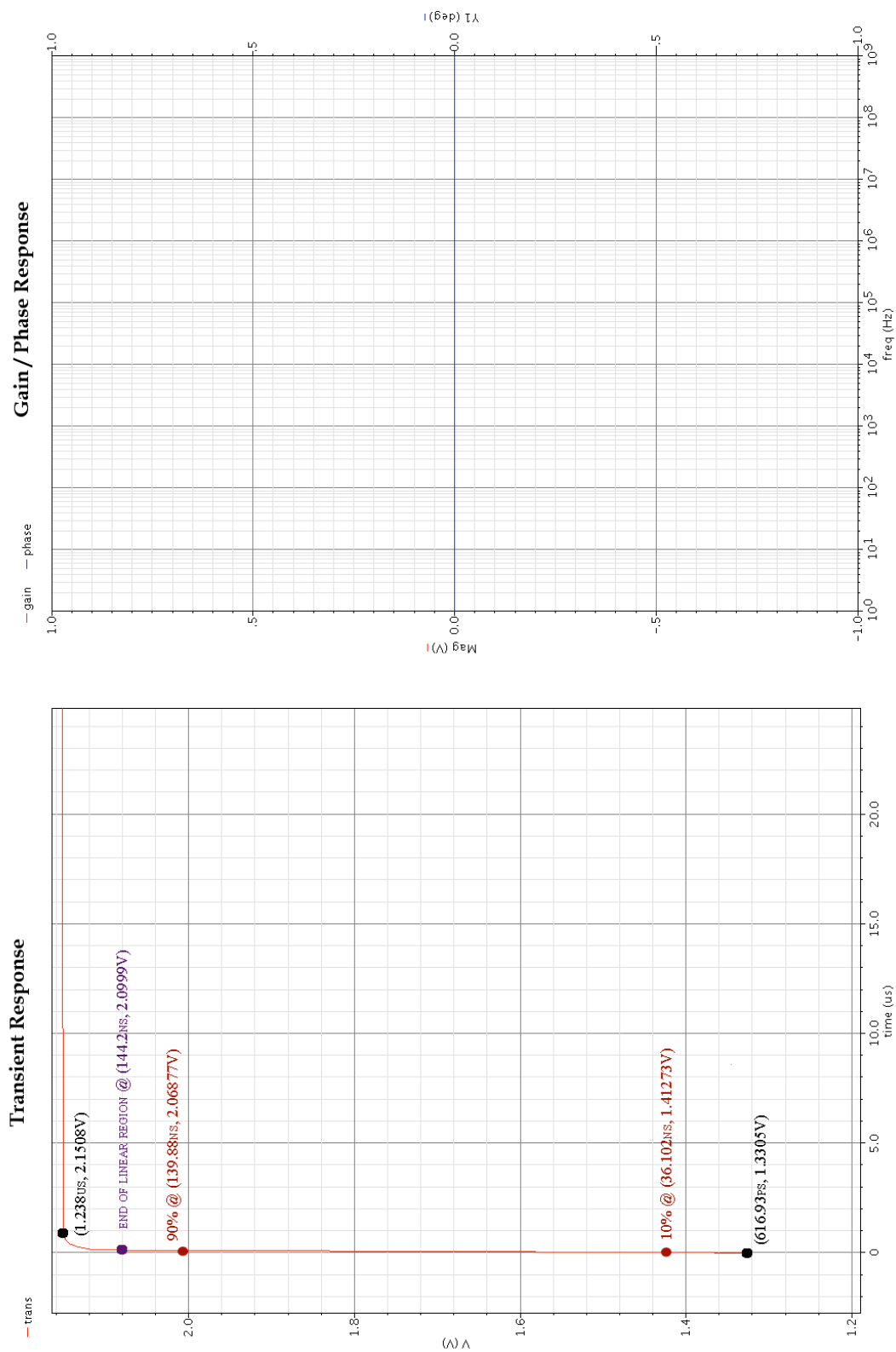


Figure #16: Slew Rate

5. Design Analysis

5.1 – Values and Concepts Analysis

A unity gain buffer amplifier is constructed by applying a negative feedback to an op-amp by connecting its output to its inverting input, and connecting the signal source to the non-inverting input. In this configuration, the entire output voltage is placed contrary and in series with the input voltage. This means the two voltages are subtracted according to Kirchoff's voltage law (KVL) and their difference is applied to the op-amp differential input. This connection forces the op-amp to adjust its output voltage to the input voltage. This circuit is often used when a voltage source with high internal impedance is used, and we want to draw more current than the source can deliver.

The process of overcoming the problems associated with frequencies in an amplifier is called frequency compensation. It usually has two primary goals: to avoid the unintentional creation of positive feedback, which will cause the amplifier to oscillate, and to control overshoot and ringing in the amplifier's step response. A compensation capacitor was added to the output of our design in order to alter the phase margin. A value of 1pF was preferred, but due to not enough phase-shift it was gradually increased to 3.5pF. Instabilities and overshoot due to capacitive loading often occur. A capacitor at the output of our circuit creates a time lag of the output voltage, because the capacitor has to be charged first. This means that the voltage at the (–) input of the op-amp is delayed too, which can cause the signal at the (+) and (–) input at certain frequencies to be 180 degrees out of phase rather than in-phase. If this happens with certain capacitance value at frequencies well above the frequency where the op-amp has an amplification less than or equal 1, this is no problem, but when this happens at a frequency where the op-amp is still capable of amplifying the signal, the circuit has been effectively turned

into an oscillator. The result is then at least overshoot or ringing at the output, and in extreme cases sporadic or continuous oscillations. If the capacitor value is large enough, this effect disappears again, with a dramatically reduced bandwidth as a result. By placing the output stage outside the feedback loop in a high voltage amplifier design this effect is circumvented.

Slew rate is the maximum rate of change of the output in V/ μ s, the number of volts that the output can rise (or fall) in one microsecond. Slew rate is used to help identify what is the maximum input frequency and amplification applicable to the amplifier such that the output is not distorted. It normally is the time an amplifier needs to go from 10% to 90% of the total output voltage in response to a step in voltage at the input. This spec limits the capability of an amplifier to generate high voltage pulses with sharp rising and falling edges, but is also a bandwidth-limiting factor for sine-wave or arbitrary signals. The highest rate of change in the output voltage of a sine wave is at the 0V-crossing. The higher the frequency, the faster the voltage has to rise there to prevent distortion of the sine wave. If the high voltage amplifier cannot follow due to its limited slew rate, the sine wave will be distorted and its amplitude is lower than at low frequencies. The maximum peak to peak sine wave output voltage V_{pp} is

related to the slew rate S_r by $V_{pp} = \frac{S_r}{\pi \cdot f}$, where f is the frequency of the sine wave, hence $S_r = V_p \cdot \pi \cdot f$. To calculate our slew rate (dv/dt) we replaced V_{ac} with V_{pulse} , in order to give a large voltage step at the input (rail to rail), and then measured the slope of the output waveform. With the measured output transient graph, there are several ways to approach calculating the slew rate: the slope over the 10%-90% region, 0%-90% region, or straight linear region. Normally in order to compensate, the slope from 10%-90% is used, but due to the sharp start of the transient signal, that does not seem applicable. Next could be the slope over 0%-90%, however this does not cover the entire change region. This leaves the slope over the linear

region, ending with a slew rate of approximately $5.3\text{V}/\mu\text{s}$, and zero phase change and gain. All variations of slew rate can be seen in Figure #4. As this is a non-inverting amp it makes sense that there is no phase shift or gain, as shown in the graphs of Figure #14 and Figure #16. With the step change, as the input is the same as the output there would be no change as well, giving a flat-line signal.

5.2 – Quality of Design

When determining the quality of design, first we look at if the circuit met the design specifications. The designed circuit met all the specifications with: $V_{DD} = 3\text{V}$; maximum power usage = 1mW with an efficiency of 4.05% ; minimum linear output swing of 1.5V with actual of 2.699V ; minimum voltage gain > 300 at 100kHz with actual of over 300 in each case; a base minimum phase margin of 45° with actual varying from $40\text{-}48^\circ$ for all cases. It produced a calculated slew rate of $5.3\text{V}/\mu\text{s}$. Detailed results can be seen in Figure #4, with the simulated graphs for each scenario marked with additional information as well.

Next we look at efficiency. Efficiency is usually a measure of how much of the power source is actually applied to the amplifier's output, and is used to break amplifiers into classes. Two important considerations in power amplification are power output and efficiency. Power output is measured in watts. Efficiency is the ratio of signal power output to total power input (wattage demanded of the power supply or battery). This value is always less than 1, and is typically expressed as a percentage. For our circuit we started out with an initial specification of a max power usage of 1mW . Using the current and voltage through the output leg, we ended using:

$$P = I \cdot V = (15\mu\text{A}) \cdot (2.6999\text{V}) = 4.04985 \times 10^{-5}\text{W} .$$

This resulted in a power efficiency of:

$$P_{eff} \% = \left(\frac{4.04985 \times 10^{-5} \text{ W}}{1 \times 10^{-3} \text{ W}} \right) \cdot 100 = 4.04985\%$$

The overall efficiency is not terribly high, hence this amplifier would possibly classify as a “Class A” inefficient op-amp.

The large signal bandwidth shows what the output amplitude voltage of a high voltage amplifier is for a given input sine wave amplitude as a function of frequency that drives it to its maximum output voltage. Because the output voltage falls off gradually above a certain transition frequency, “the bandwidth” is only useful if also the reduction of the full-power bandwidth of the high voltage amplifier at this frequency is also quoted. This is often expressed as the -3dB point, where the amplitude has fallen to 0.707 times the maximum amplitude at low frequencies, however this is not always the way it is specified. The small-signal bandwidth, also sometimes called “the bandwidth”, is the frequency response of the high voltage amplifier at some very low output voltage like 1% of the maximum output. This bandwidth is usually larger than the large signal bandwidth by a significant amount. The frequency where the signal begins to decrease may also be considered the bandwidth as well. For this experiment, the beginning and end of the curves are listed under the bandwidth of Figure #4 (and documented on the measured graph results), and the -3dB and 1% point listed under the gain calculations. In order to calculate the phase either the -3dB point or the 1% can be used. In Figure #4 both points are calculated and measured, however as we are measuring the small signal gain, the 1% point is used to calculate the phase for each scenario.

Operational amplifiers often have a very high gain, with the current saturating at higher V_{ds} , so small drain current variations can cause large drain voltage variations. Gain is normally defined as the ratio of the output to the input of the amplifier. In the operational amplifier, we

have a relationship between the output voltage and the input voltages at the input terminals of the operational amplifier. We can notice a correlation between the gain and the bandwidth where the higher the gain, the lower the bandwidth. From the simulation scenarios run, we can see that using body effect gives us better gain and using unity slightly decreases our gain. In equations #7, #8, and #9 we can see the relationship between overvoltage, current, and W/L when calculating gain. To achieve large values of gain, we must choose the correct balance of values, so as not to over or under compensate. We chose: low V_{ov} , medium current, and high W/L ratios running through leg I2; high current, and high W/L ratios running through leg I1.

6. Conclusion

We were given a set of design specifications and told to design an op-amp. To create a high speed high voltage amplifier for a certain purpose, one has to look not only at the bandwidth and/or slew rate of the amplifier, but also at the expected capacitive load, the maximum sustainable output current and the possibility of overshoot voltages damaging the load. All of these are required for an optimal result. Our designed circuit met the specifications: $V_{DD} = 3V$; maximum power usage = 1mW with an efficiency of 4.05%; minimum linear output swing of 1.5V with actual of 2.699V; minimum voltage gain > 300 at 100kHz with actual of over 300 in each case; a base minimum phase margin of 45° with actual varying from $40-48^\circ$ for all cases; measured slew rate of approximately 5.3V/ μ s. Detailed results can be seen in Figure #4, with the simulated graphs for each scenario marked with additional information as well.

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